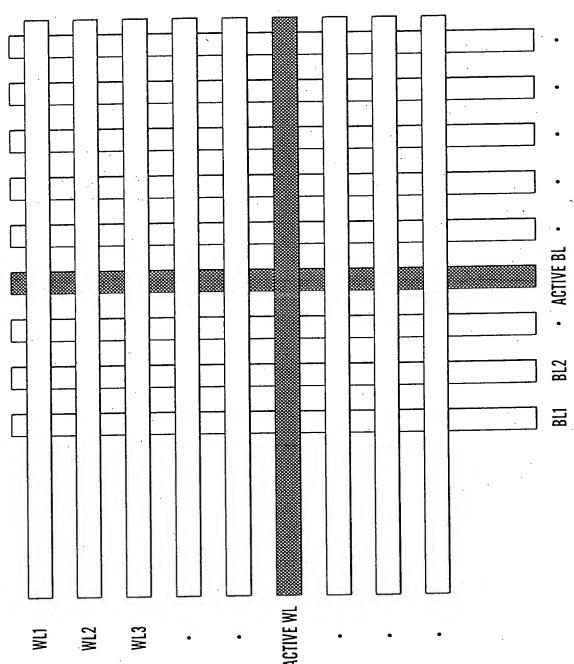


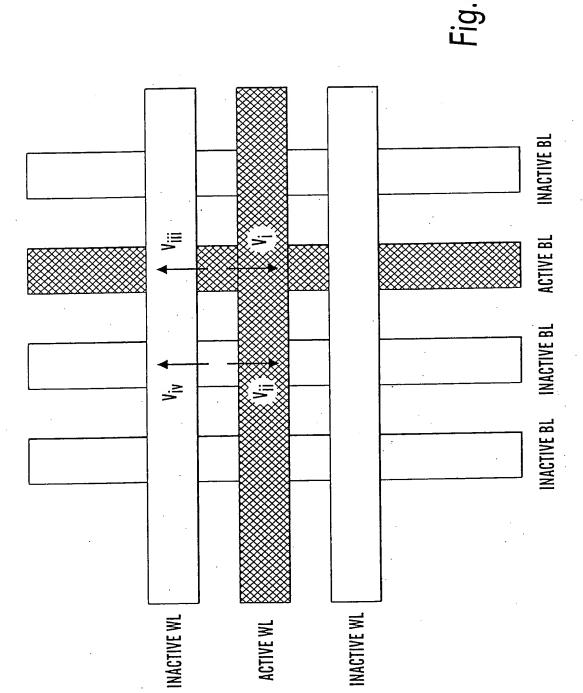
Fig. 1



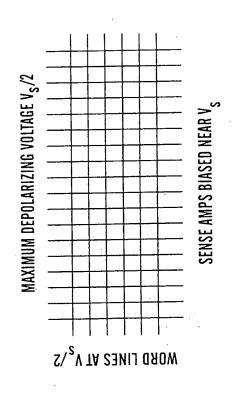


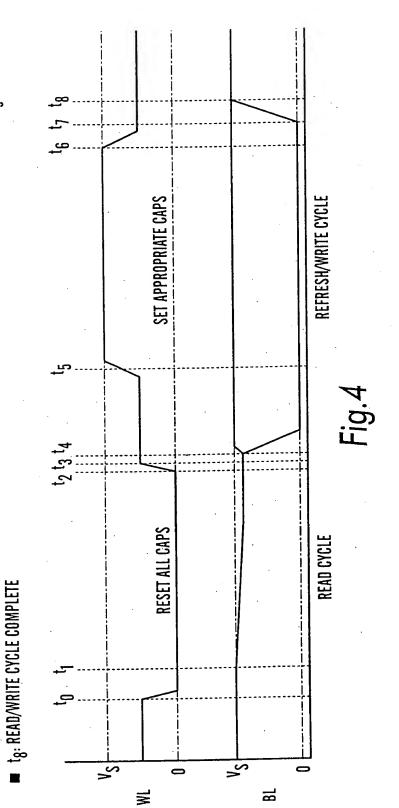








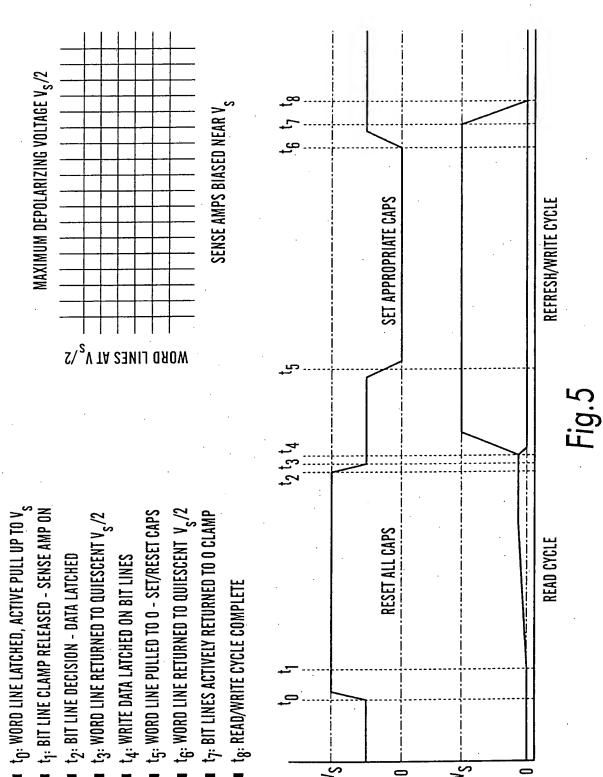




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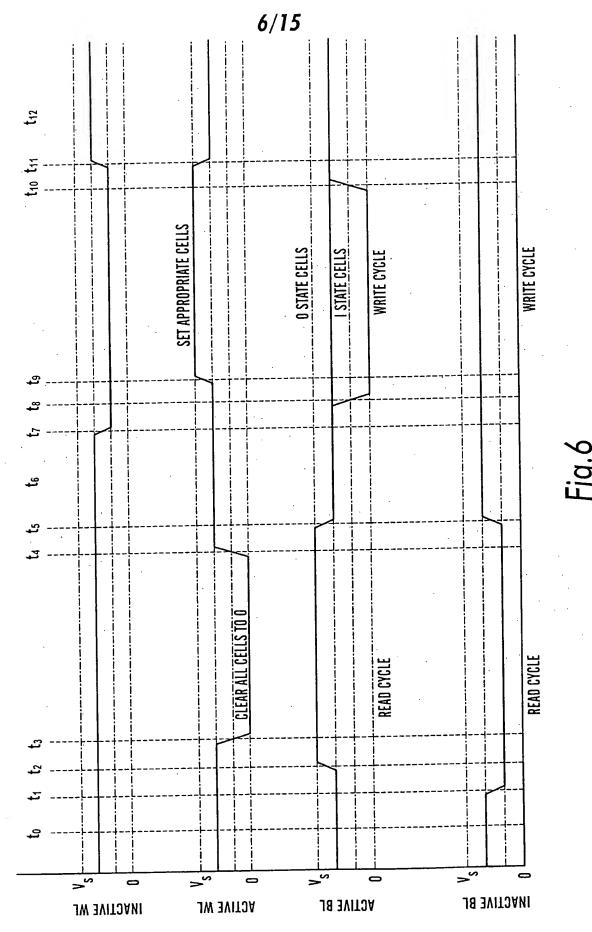
 \mathfrak{t}_0 : word line latched, active pulldown to 0 $t_{\rm S}$: Word line pulled to V $_{\rm S}$ - Set/reset caps $\mathbf{t_{7}}$. Bit lines actively returned to $\mathbf{v_{S}}$ clamp t_{6} : Word line returned to quiescent $v_{c}/2$ t_{\uparrow} : Bit line clamp released - sense amp on \mathfrak{t}_3 ; word line returned to quiescent $v_{\mathfrak{e}}/2$ \mathfrak{t}_2 : bit line decision – data latched $\mathbf{t_4}$: Write data latched on bit lines



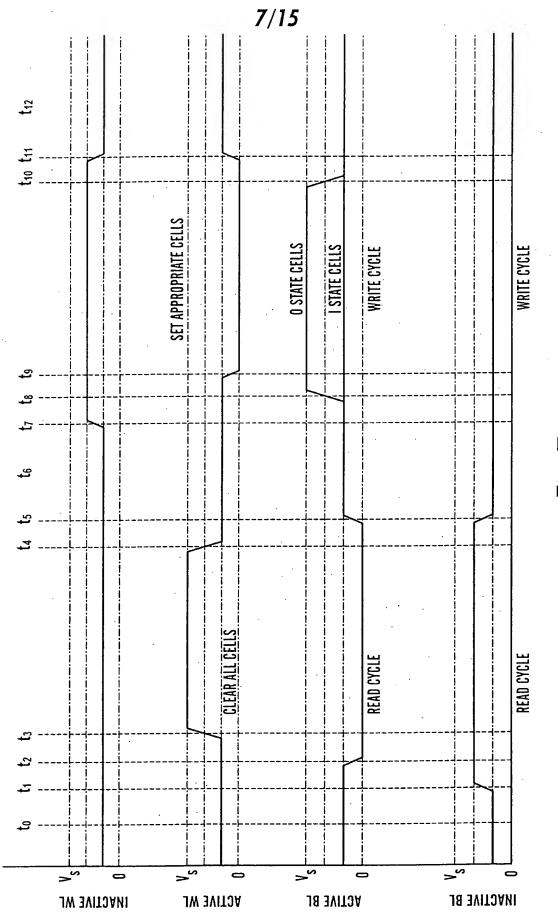


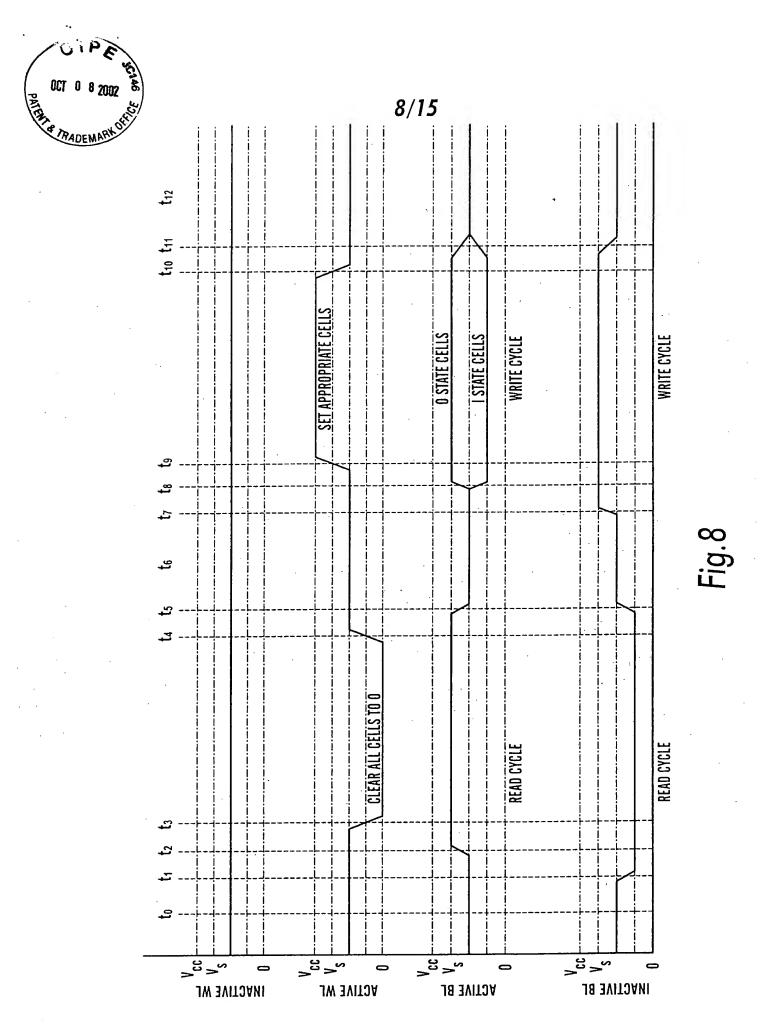
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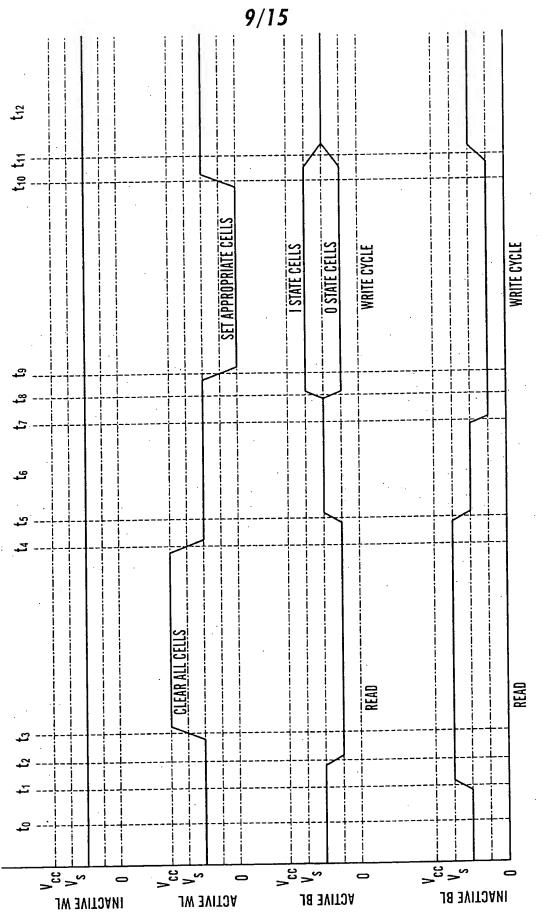


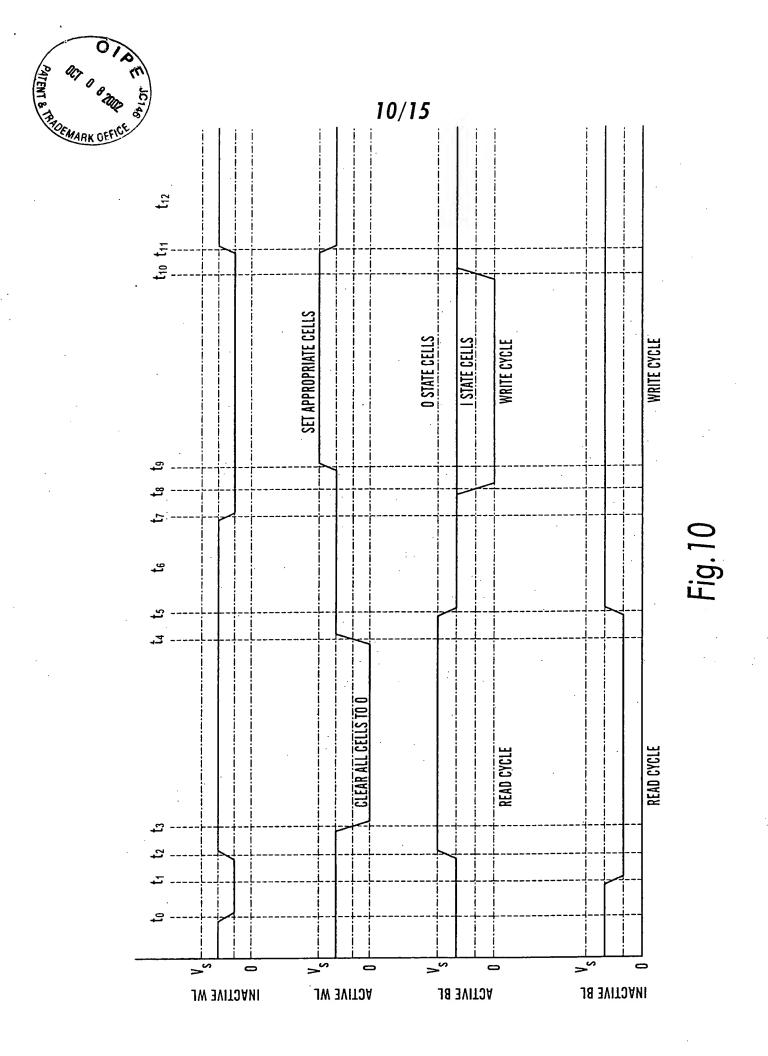


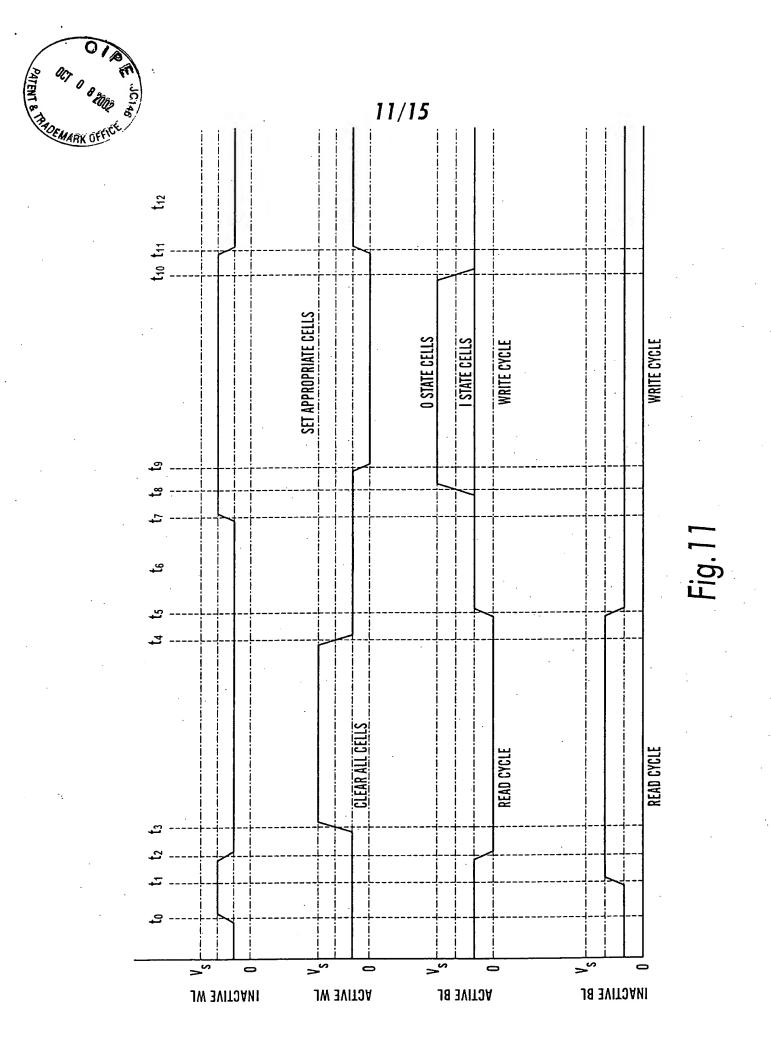


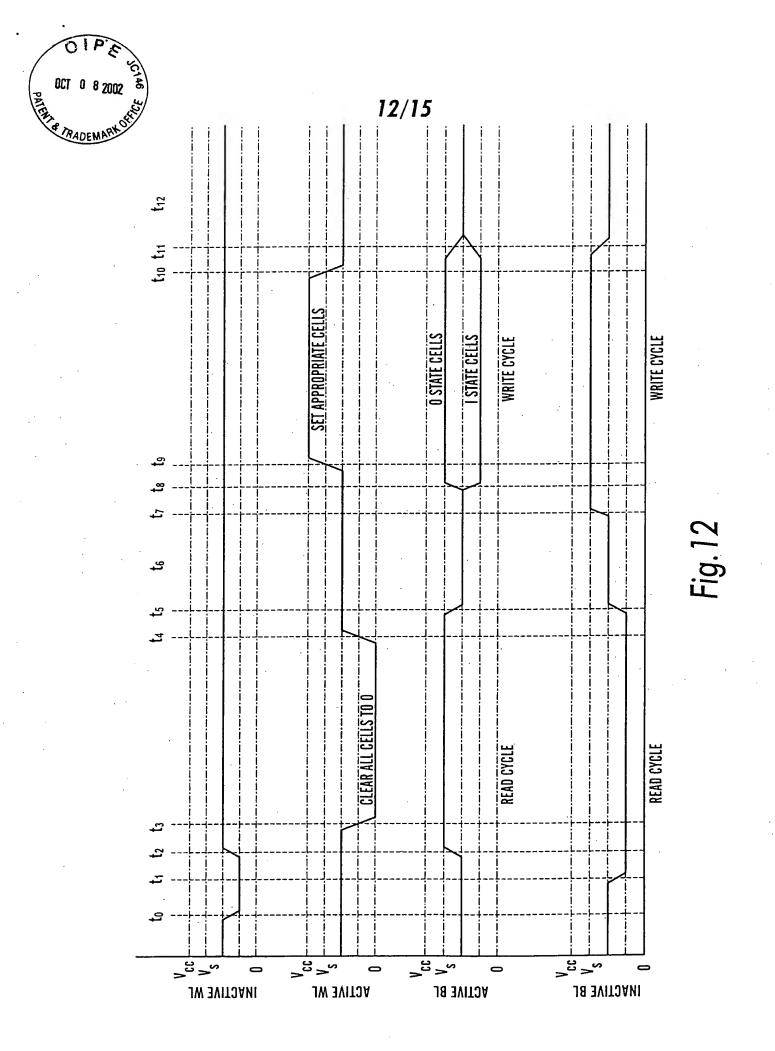




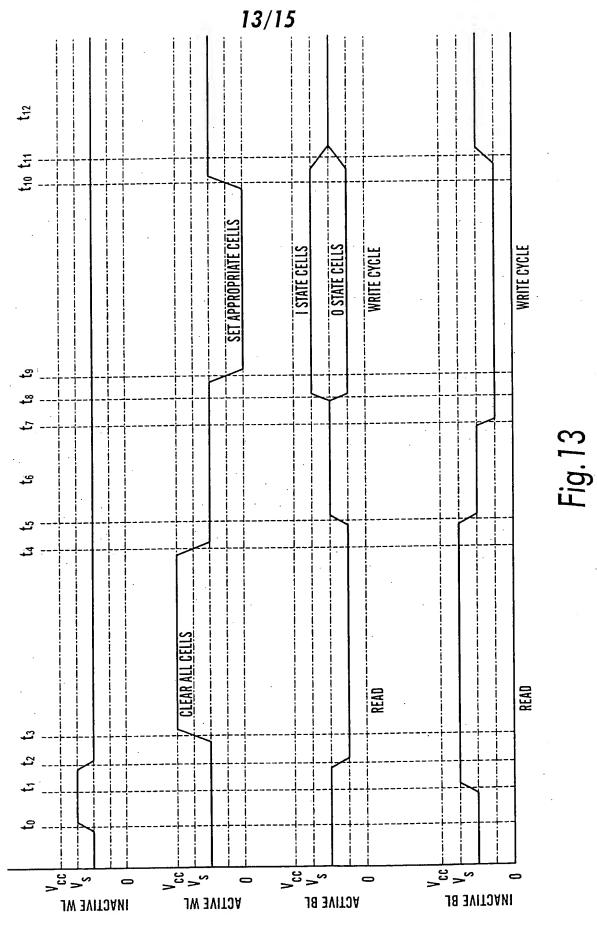














EXAMPLE OF READ AND WRITE PROTOCOL INVOLVING A PRE-READ REFERENCE CYCLE

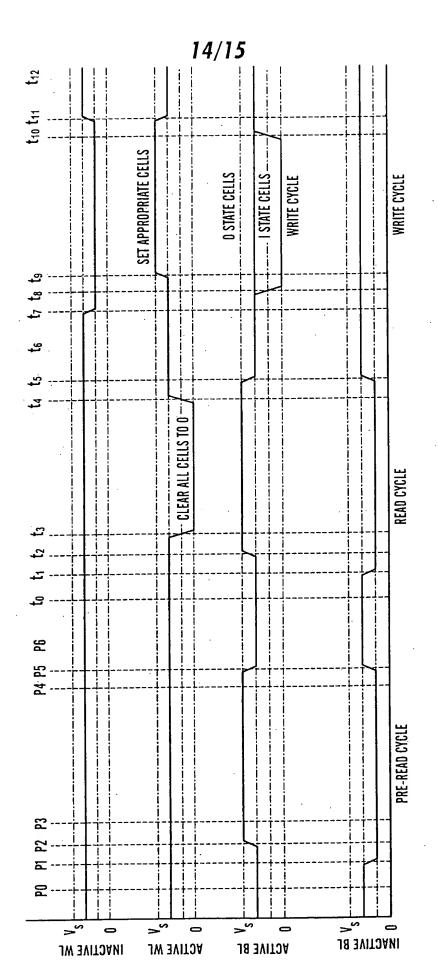


Fig. 14



